ABSTRACT

The present invention allows an efficient test as to the presence of line defects in data lines and gate lines in a liquid crystal display. A logic circuit for a test is provided according to the interconnect layout structure on a semiconductor substrate of a liquid crystal display, and ends of data lines are coupled to inputs of the logic circuit. At the time of the test, test drive signals corresponding to a certain logical value are applied to the data lines, and a determination is made as to defects in the data lines based on the output from the logic circuit, obtained in response to the signal application. This way means that determinations can be made as to defects in the data lines based on a logical value as the output from the logic circuit, i.e., binary values. Such a configuration is also applied to gate lines.